Integrated Power Management with Switched-Capacitor DC-DC Converters

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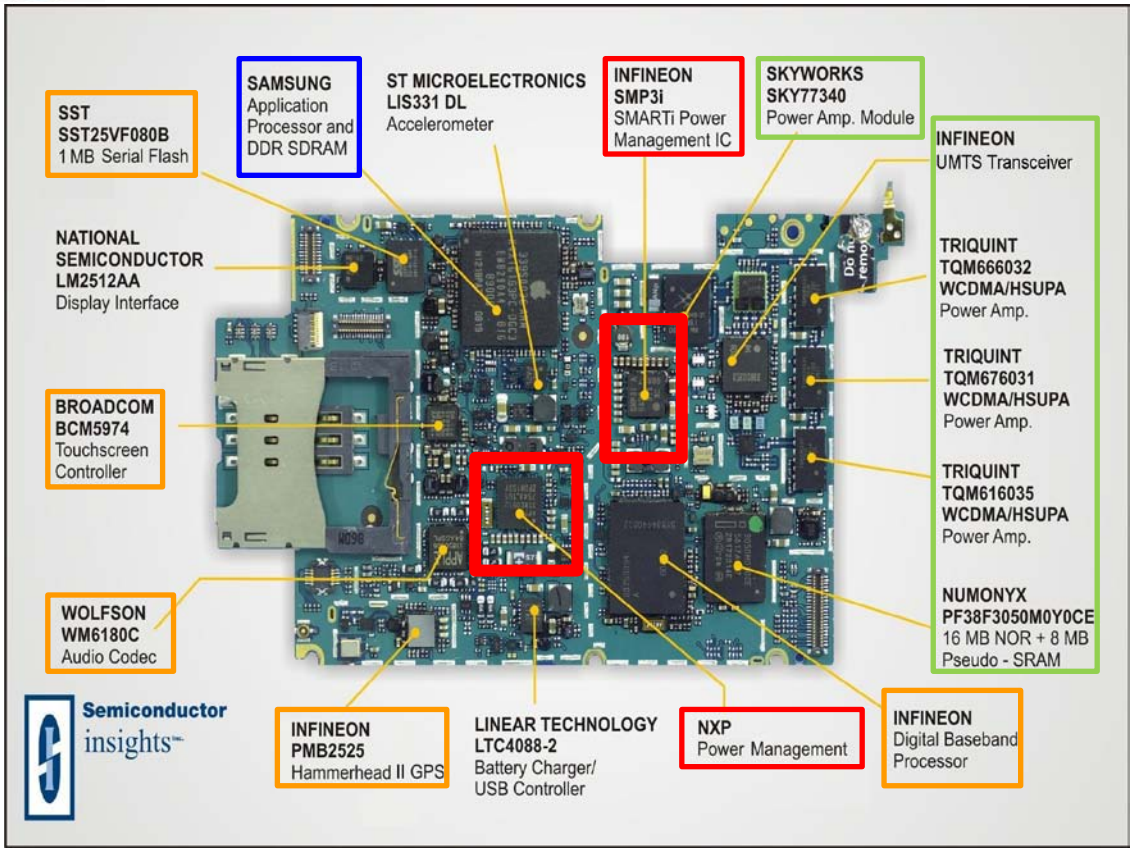
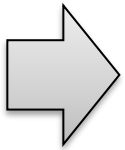
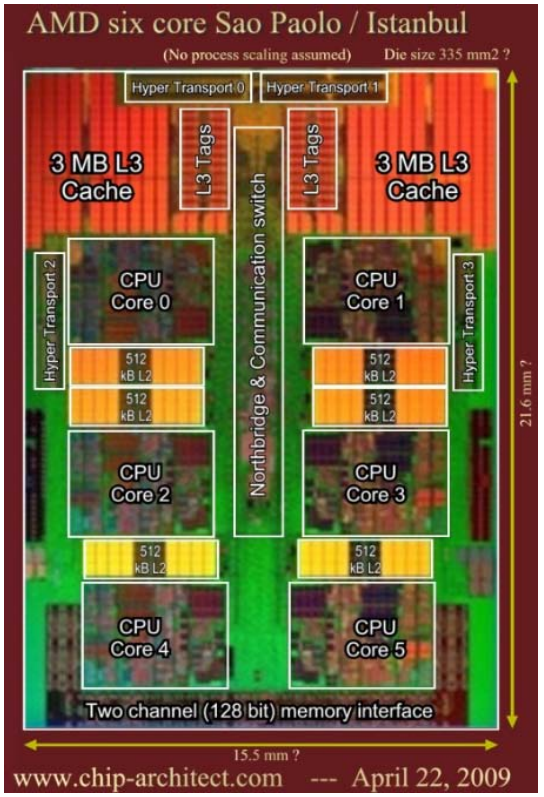
Integration Challenges



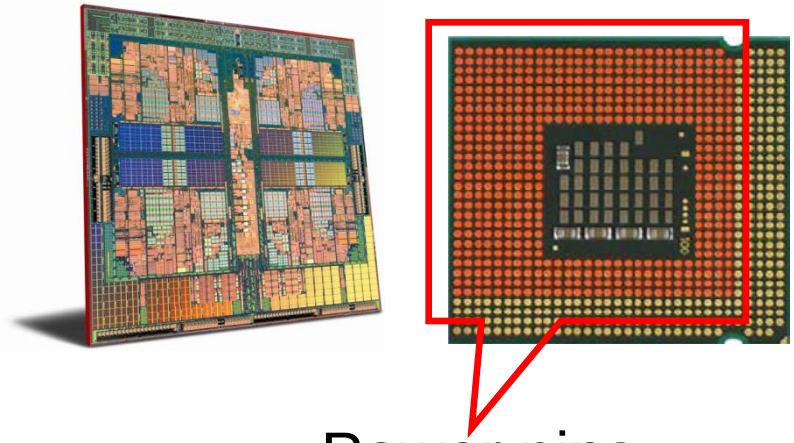


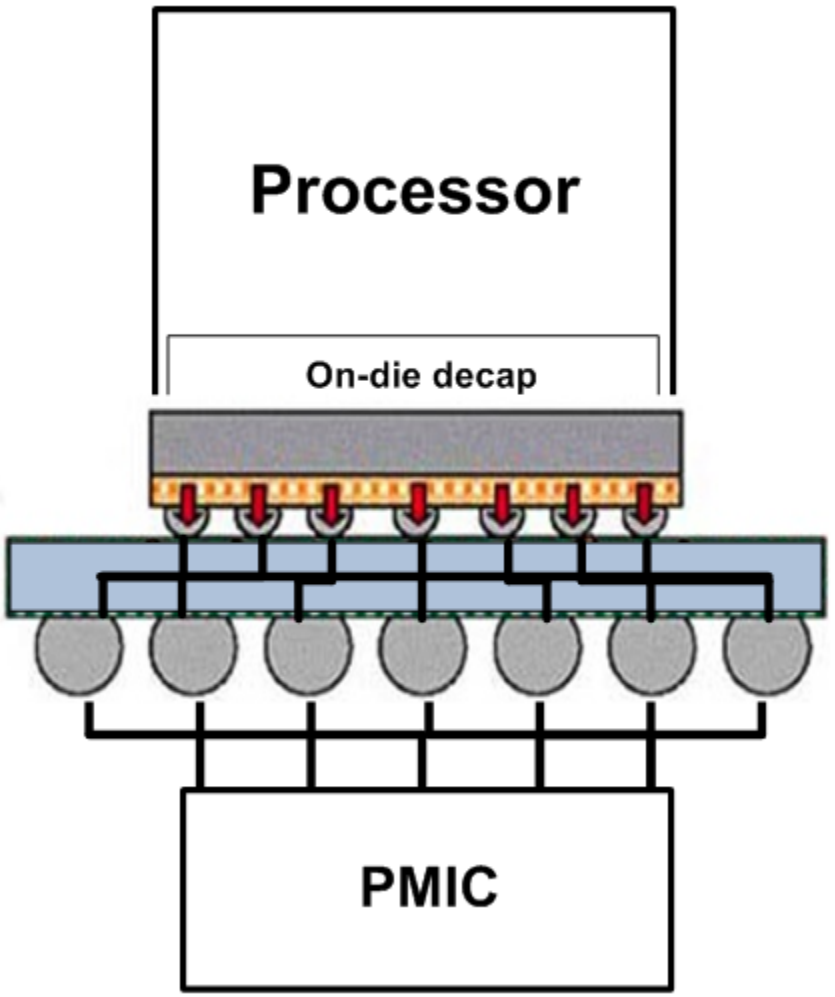


- **Integration has a benefit in energy efficiency**
  - Save IO power, board area

- **But it has a problem**
  - Need different voltage supply for different blocks/IPs and different modes of operations (DVS).

Limited Resources



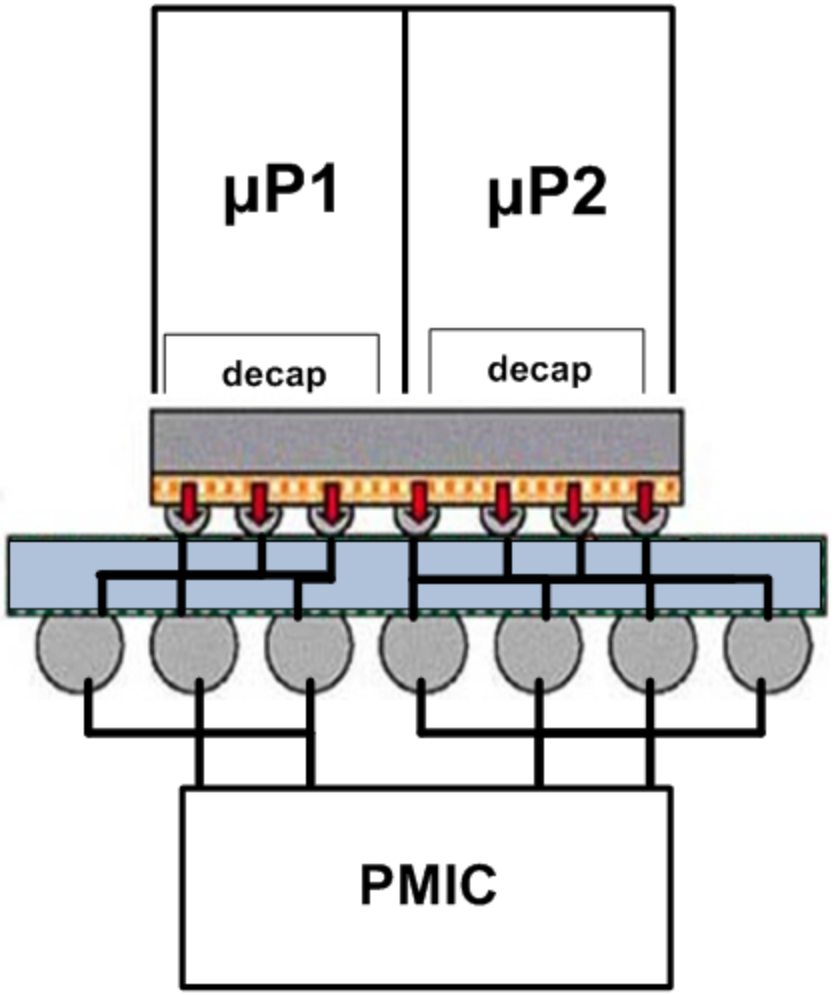


- **Functions on-die increases the need for separate supply**
- **But the resources (pins and decap) are limited**

Multiple Off-chip Supplies: Not Appealing

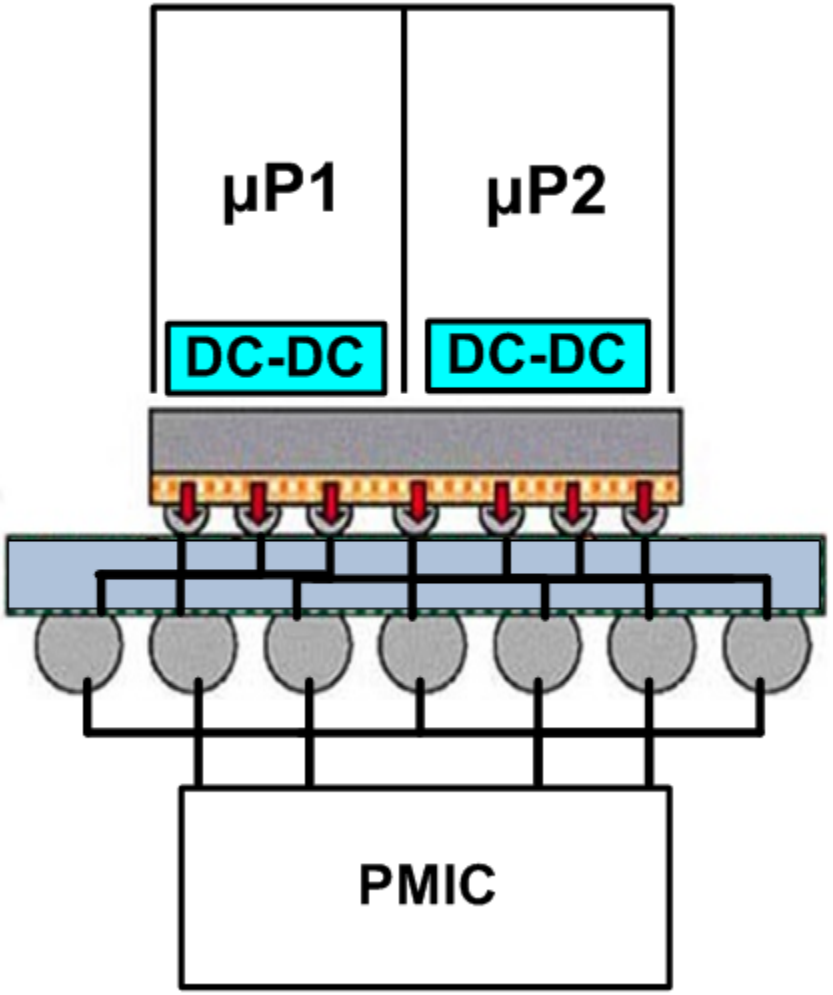
- Split power plane leads to supply impedance degradation
- Compensating by de-cap is area-consuming → costly solution

→ Just supplying power from off-chip is not appealing



Integrated DC-DC Converters

- **One global supply onto die**
  - Local power generated by fully integrated DC-DC converters
- **Don’t lose anything from package side**



→ How to make integrated DC-DC conversion efficiently?

Outline

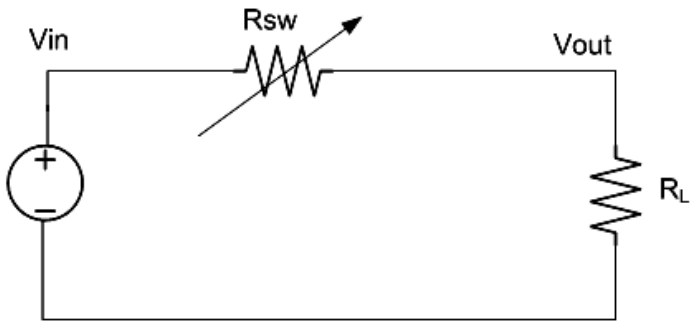
- Motivation

- Integrated converter efficiency
  - Choice of energy storage element
  - Efficiency analysis

- Switched-capacitor converter design and prototype

DC-DC Converter: Linear vs. Switching

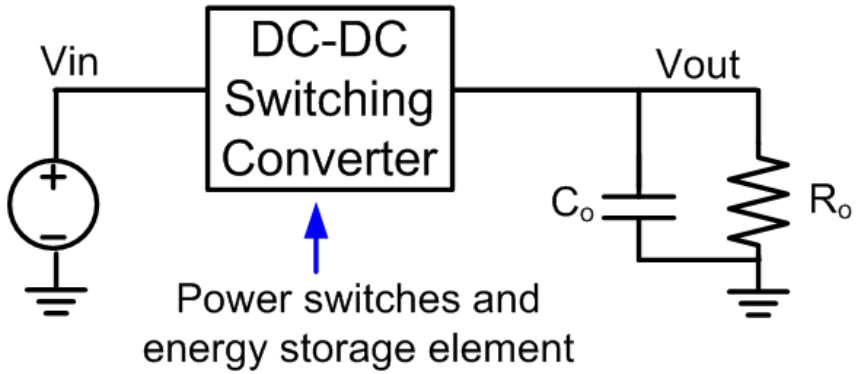
Linear Regulator



$$\eta = \frac{V_{out}}{V_{in}}$$

- Fundamental limit on efficiency

Switching Regulator

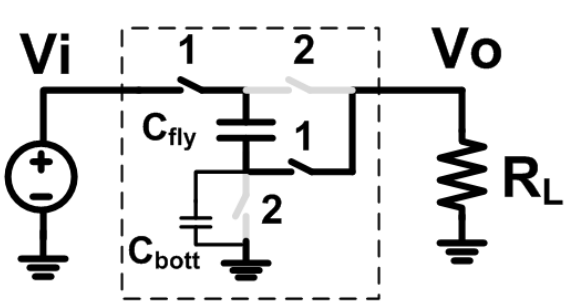


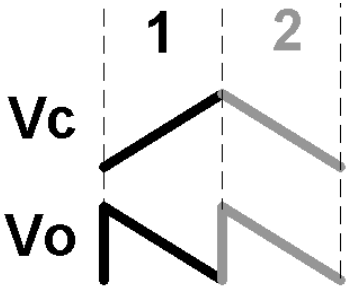
Inductor or Capacitor?

- Efficiency is ideally independent of conversion ratio.
- Theoretically, can reach up to 100% efficiency

SC – Operation of 2-to-1 Conversion

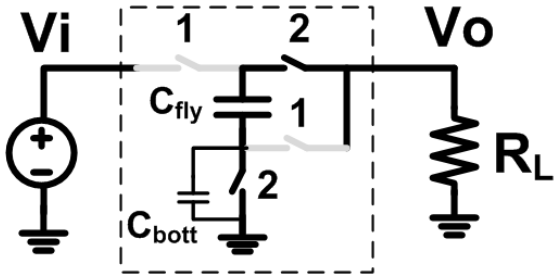
Phase 1

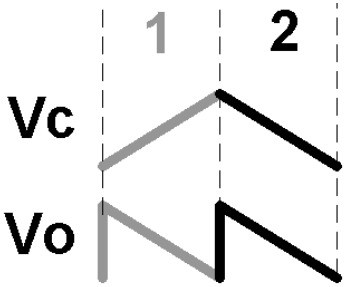




- Two-phase operation
  - Phase 1: charge capacitor

Phase 2





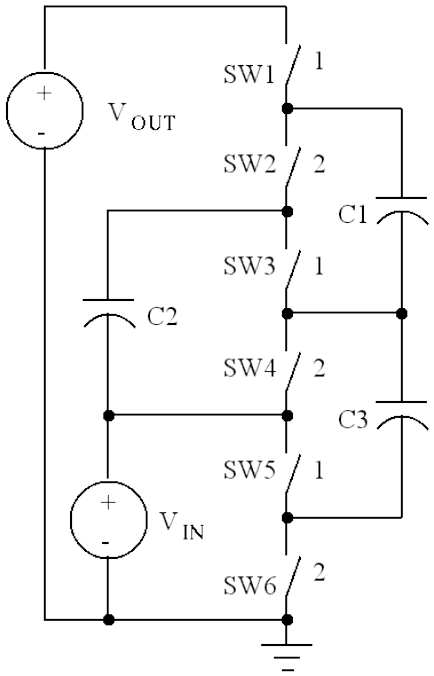
- Phase 2: capacitor transfers charge to output

- Equivalent resistance from loss over switched-cap

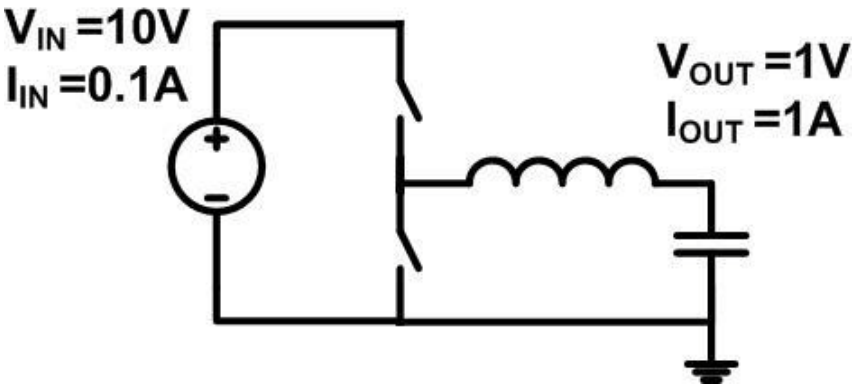
$$R_{switched\text{-}cap} = \frac{1}{M_{conv,cap} f_{sw} C_{fly}}$$

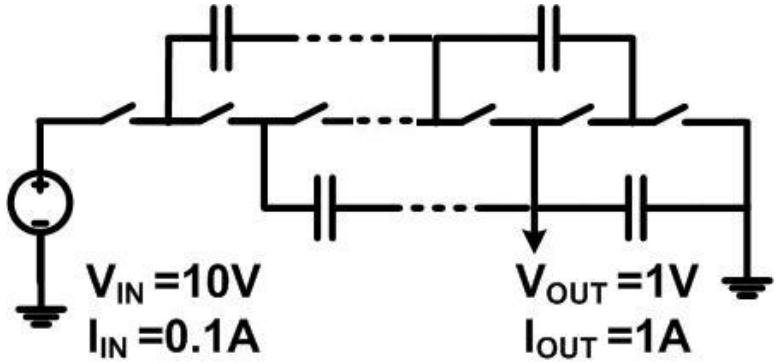
Switched Capacitor Power Converters

- **Only switches and capacitors**
- **Using no inductors has advantages:**
  - Simplified full integration potential
  - Works well over a wide power range
    - Single mode, can adjust clock rate
    - No minimum load
  - No inductive switching losses
- **Open-loop loadline regulation possible:**
  - Output impedance has R-C characteristic, with R naturally designed to meet efficiency spec



First Look





Magnetic boost/buck:

- 10-to-1 V conversion, 1A @ 1V
- S1,S2 rated for V-A product of V*I = 10 V-A
- Sum up to 20 V-A
- Need inductor, inductor loss,
- Inductive switching

10-to-1 Ladder Switched-Cap:

- 10-to-1 V conversion, 1A@1V
- 20 switches, each blocks 1V
- 18 switches handle 1/5 A
- 2 switches handle 9/5 A
- V-A product sums up to 36/5 =7.2 V-A
- Intrinsic CMOS device convenient

The Submicron Opportunity

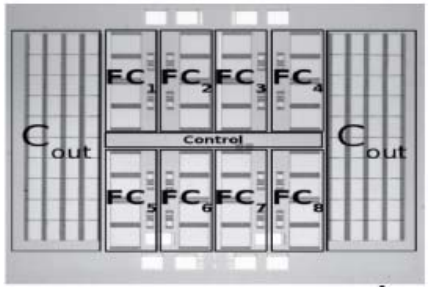
- **Rate device by ratio:** $G_s V_s^2 / C V_g^2$
  - Essentially an Ft type parameter for a power switch reflecting power gain
  - **Opportunity in scaling**

- **Suggests that we should look for opportunities to build our ckts with scaled CMOS based devices, but:**
  - Low voltage rating per device
  - Inadequate metal/interconnect for high current?

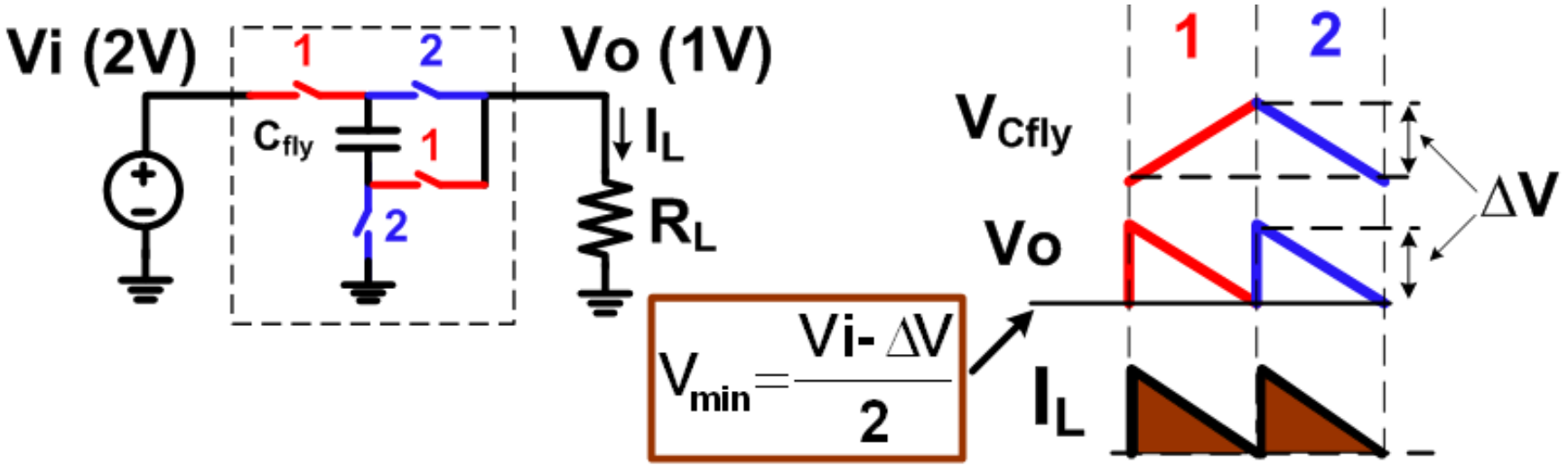
Why Not S-C ?

- Difficult regulation?
- Not suited for high current/power?
  - Magnetic-based ckts = higher performance?
- Interconnect difficulty for many caps?
- Voltage rating of CMOS processes?
- Ripple?

Previous Work

Work	[1] Breussegem, VLSI 09	[2] Somasekhar, VLSI 09
Technology	130nm Bulk	32nm Bulk
Topology	2/1 step-up	2/1 step-up
Interleaved Phases	16	32
Converter Area (mm^2)	2.25	6.678×10^{-3}
Power density @ η_{max}	2.09 mW/mm^2	1.123 W/mm^2
Efficiency (η_{max})	82%	60%
Die photo		

Switched Capacitor Loss

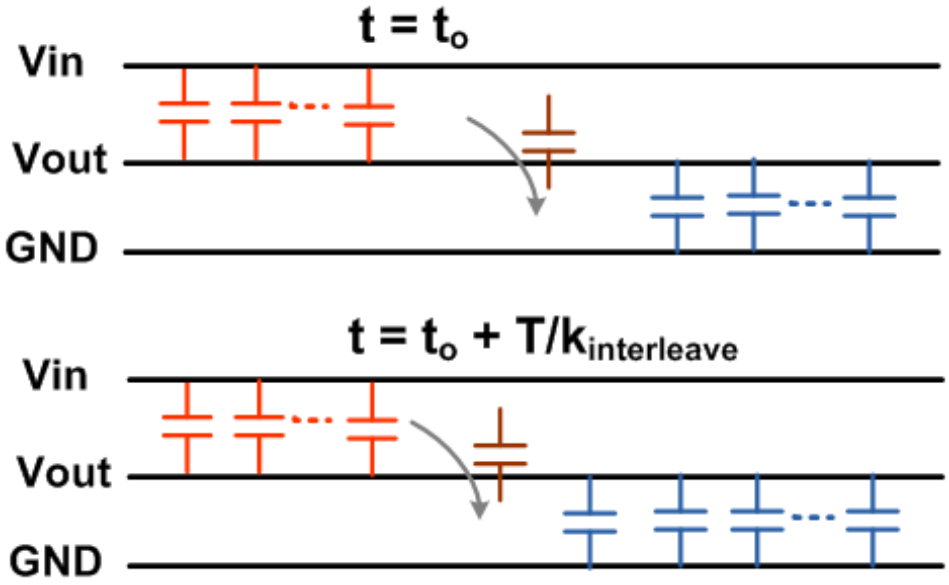


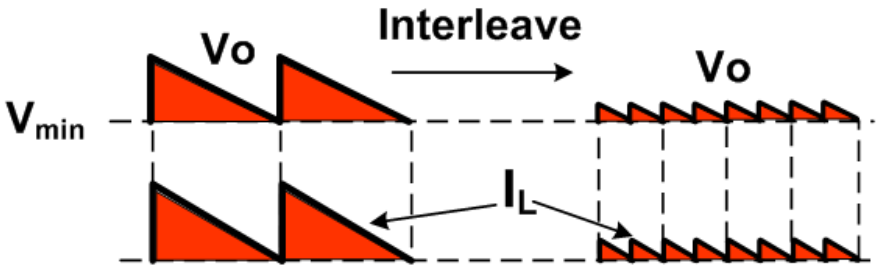
- **Converter supplies digital circuits**
  - Performance (f_{CPU}) set by V_{min}

- **Intrinsic switched-capacitor loss:**

$$P_{C_{fly}} = 2x \frac{I_L^2}{M_{conv,cap} f_{sw} C_{fly}}$$

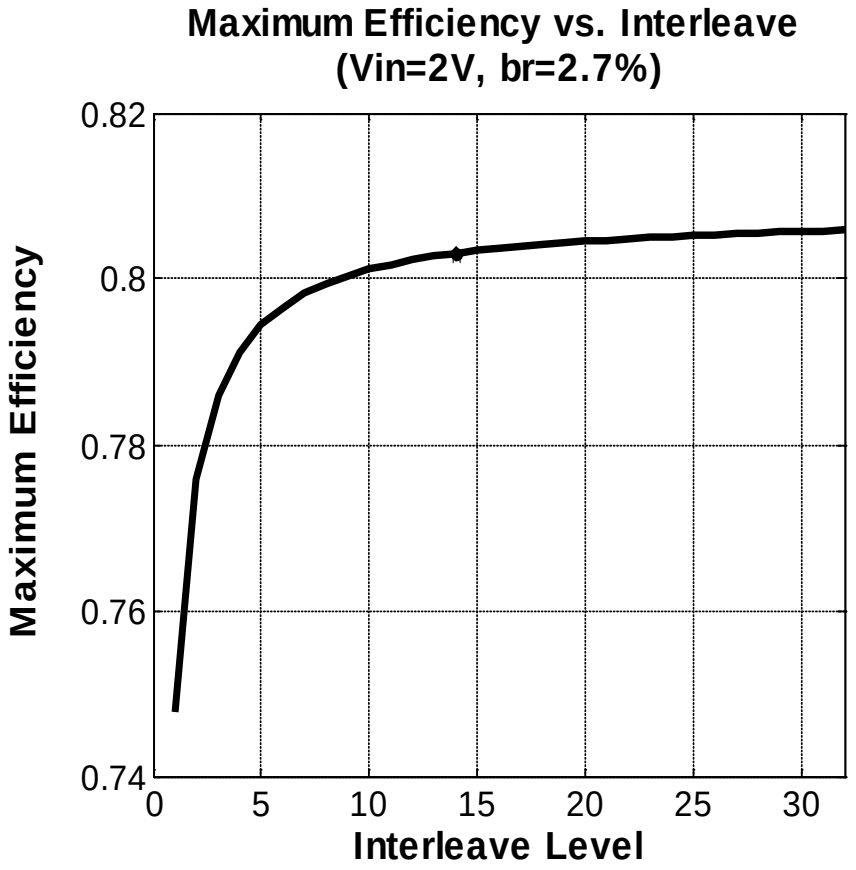
Multi-Phase Interleaving





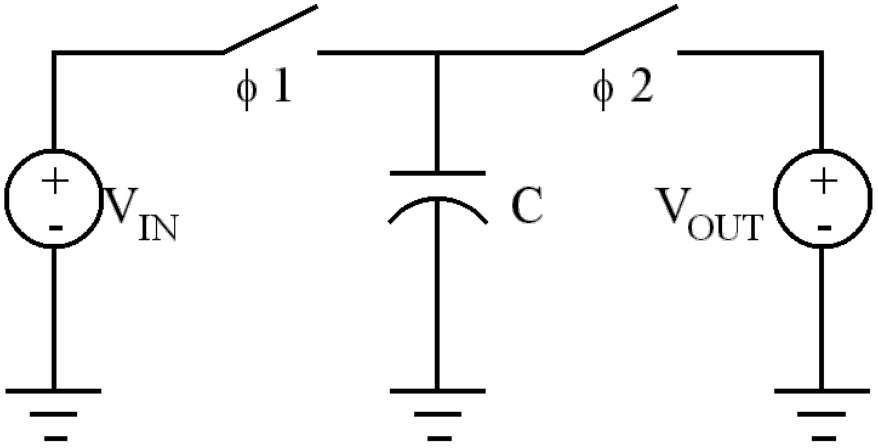
- **Good news:**
  - Interleaving can reduce ripple without changing V_{min}

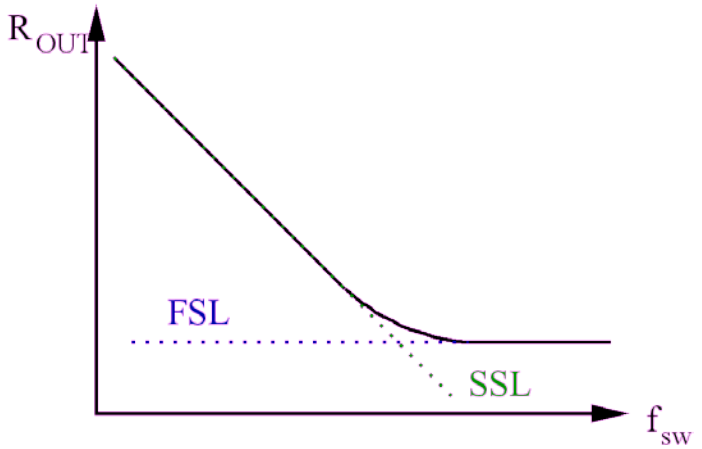
$$P_{C_{fly}} = \left(1 + \frac{1}{k_{interleave}}\right) \frac{I_L^2}{M_{conv,cap} f_{sw} C_{fly}}$$



Ref: D. Ma, F. Luo, *IEEE Trans. VLSI Sys.*, 2008

SC Analysis: Simplest Example





- **Slow Switching Limit (SSL):**
  - Impulsive currents (charge transfers)
  - Resistance negligible (assume R = 0)
  - This (SSL) impedance is the switching loss!

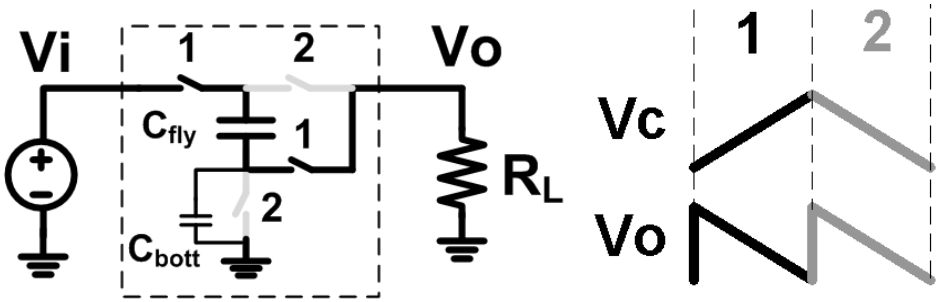
$$i = f_{sw}\Delta q = \boxed{f_{sw}C\Delta v}$$

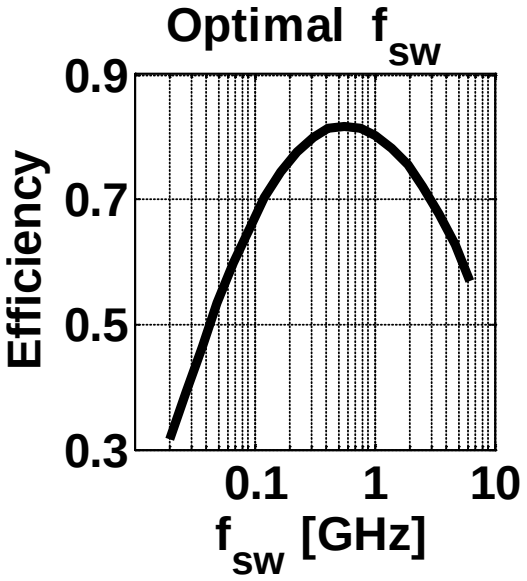
- **Fast Switching Limit (FSL):**
  - Constant current through switches
  - Model capacitors as voltage sources (C → ∞)

$$i = \boxed{\frac{1}{4}\frac{1}{R}}\Delta v$$

$$(\Delta v = V_{IN} - V_{OUT})$$

SC – Loss Optimization





- **4 main loss components**

$$P_{loss} = P_{Rsw} + P_{C_{fly}} + P_{bott.cap} + P_{gate.cap}$$

$$\alpha\ I_L^2 \frac{R_{on}}{W_{sw}} \qquad \alpha\ \frac{I_L^2}{f_{sw} C_{fly}} \qquad \alpha\ C_{bott} f_{sw} \qquad \alpha\ W_{sw} C_{gate} f_{sw}$$

Switch resist. | Switched cap | Bottom Plate | Gate loss

Series Losses (Ro) | Parasitic Losses ($R_{//}$)

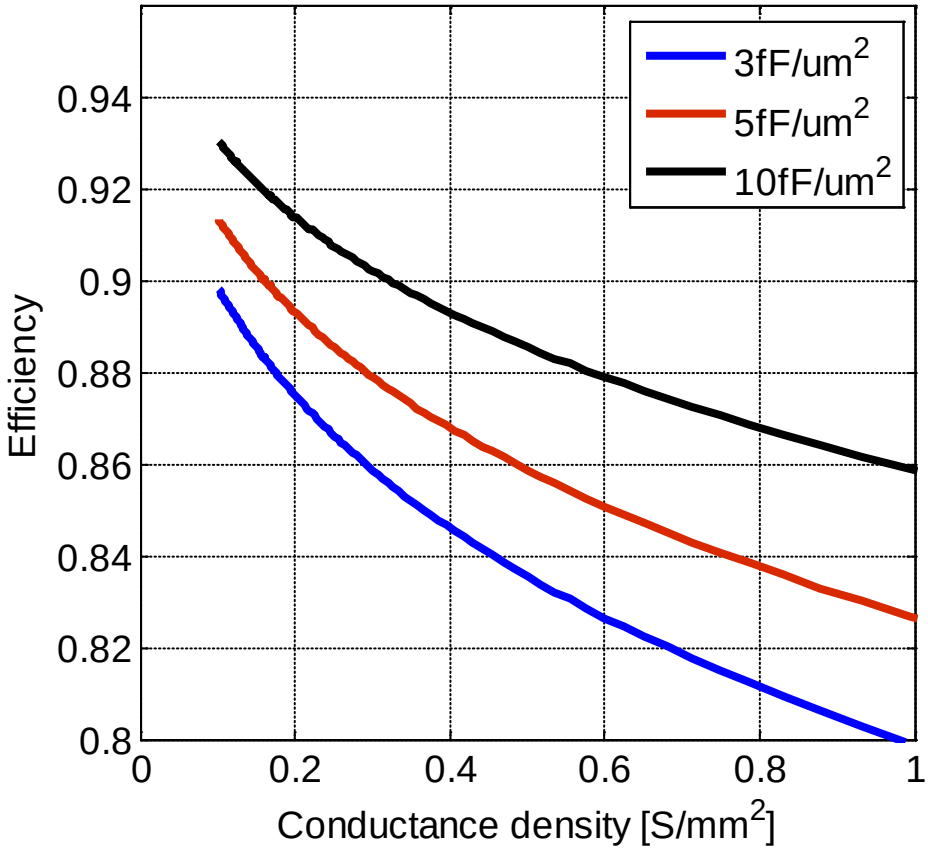
Optimization for Efficiency

$$P_{loss} = P_{Rsw} + P_{C_{fly}} + P_{bott.cap} + P_{gate.cap}$$

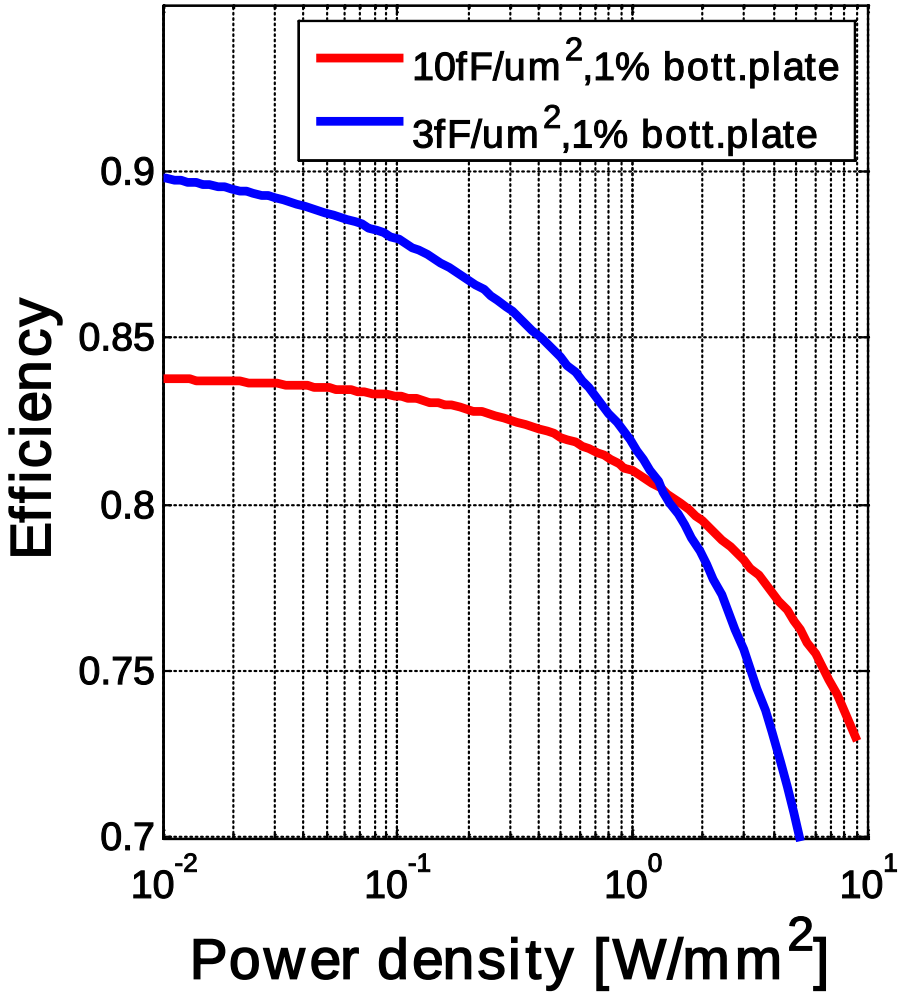
- **No bottom plate cap, optimize switch sizes W_{sw} and switching frequency f_{sw}**

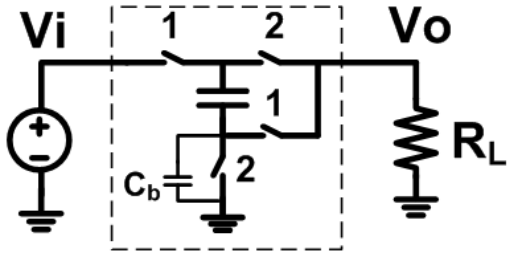
$$\frac{P_{loss}}{P_{Load}} = 3M_{conv,tech}\sqrt[3]{\frac{V_{sw}^2 R_{sw} C_{gate}}{V_o^2 R_L C_{fly}}}$$

Efficiency vs. Cap. Density



Optimization for Efficiency





- **Efficiency and Power density trade-off**
- **At lower power density:**
  - Bottom plate critical
- **At high power density:**
  - Flying cap critical

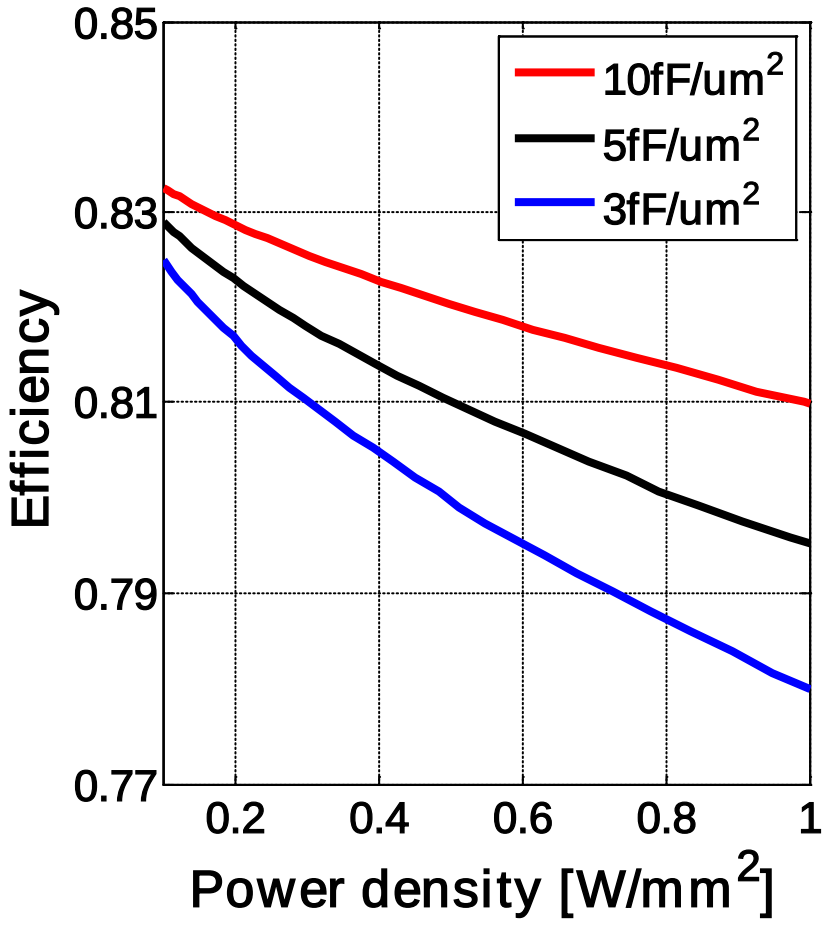
$$\frac{P_{loss}}{P_{Load}} \approx \sqrt{M_{conv} k_{bott}} + \sqrt{\frac{1}{\sqrt{M_{conv} k_{bott}}} \frac{V_{sw}^2 R_{on} C_{sw}}{V_o^2 R_L C_{fly}}}$$

Achievable Performance

- **Looks promising**
  - Especially in mobile applications
  - 1W/mm^2 converter fits in decap area
- **Only looked at 2:1 converter so far**
  - Need to support multiple output voltage levels

Eff. vs. Cap Density

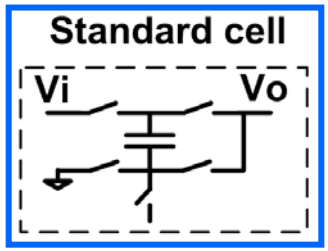
(k_{bott} = 3%)

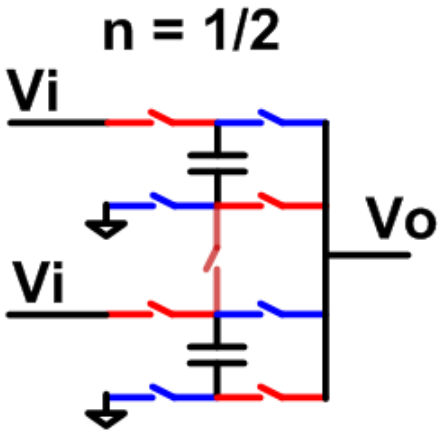


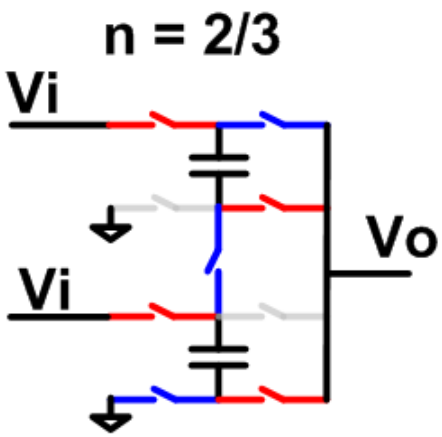
Outline

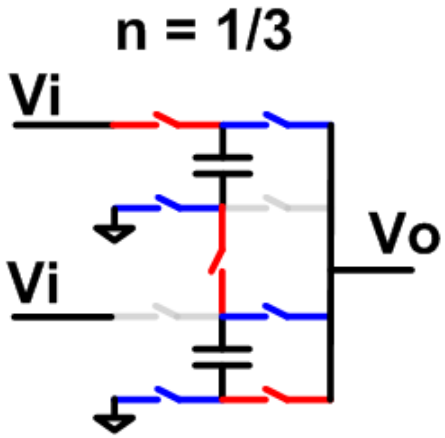
- Motivation
- Integrated converter efficiency
  - Choice of energy storage element
  - Efficiency analysis
- Switched-capacitor converter design and prototype

Multiple Conversion Ratios

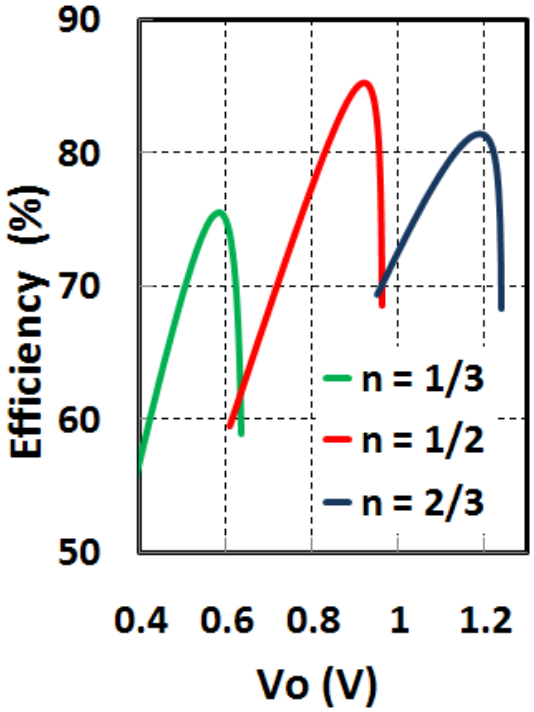






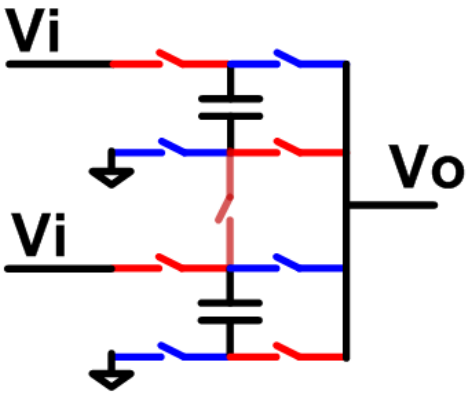


- **Standard cell design supports multiple conversion ratios**
- **Fine output voltages achieved by controlling f_{sw} (or W_{sw})**
  - Equivalent to linearly regulating down from peak efficiency
- **How to drive the switches?**

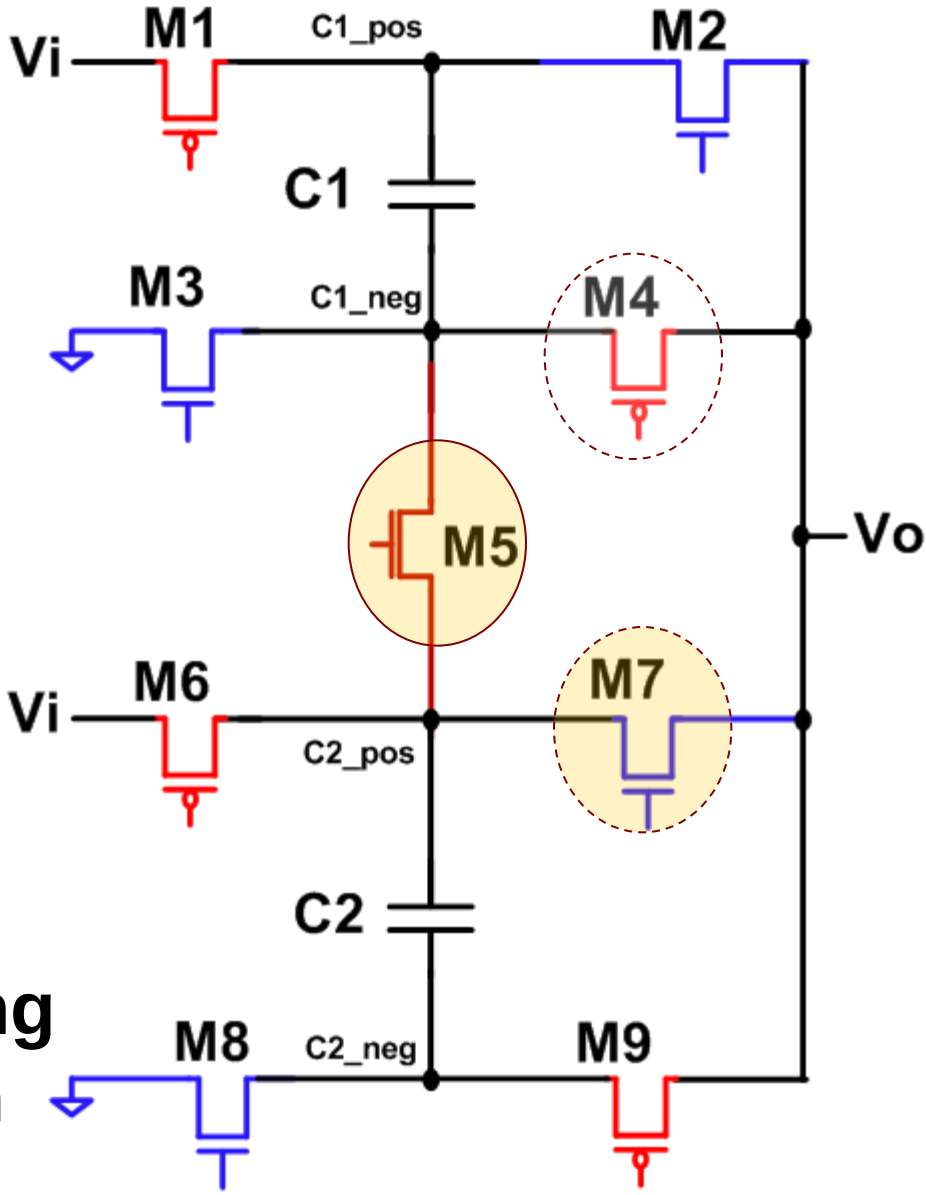


Ref: D. Maksimovic and S. Dhar, *IEEE PESC, 1999*

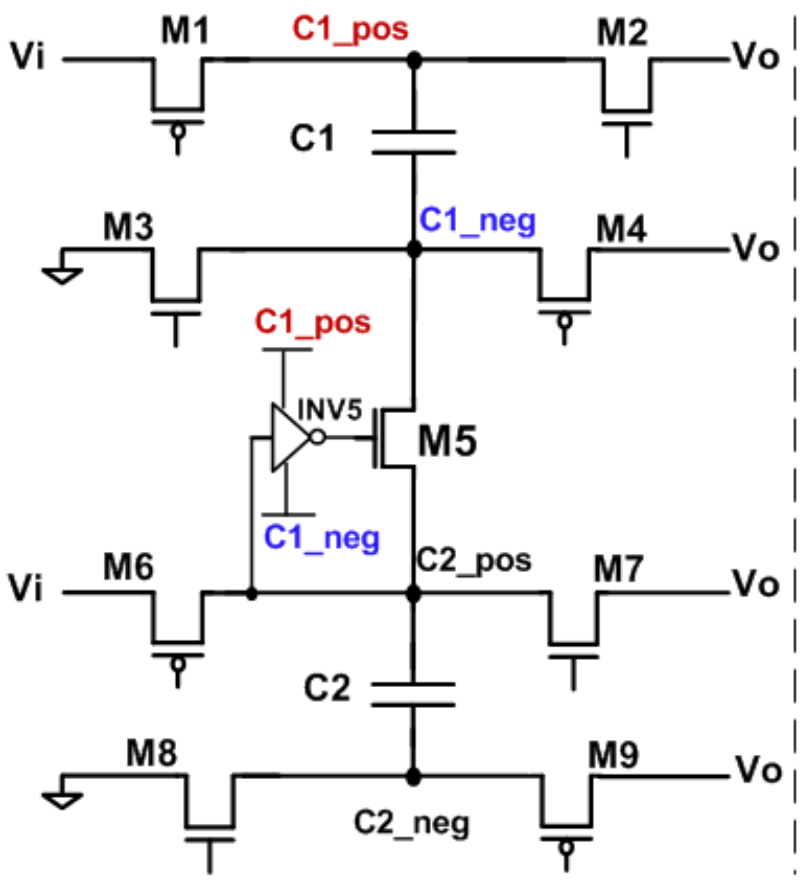
Switch Drivers

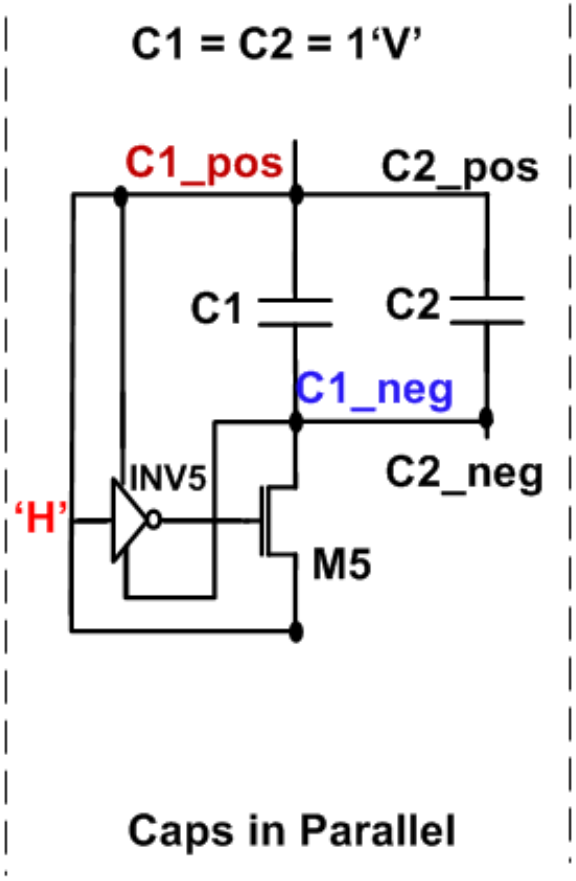


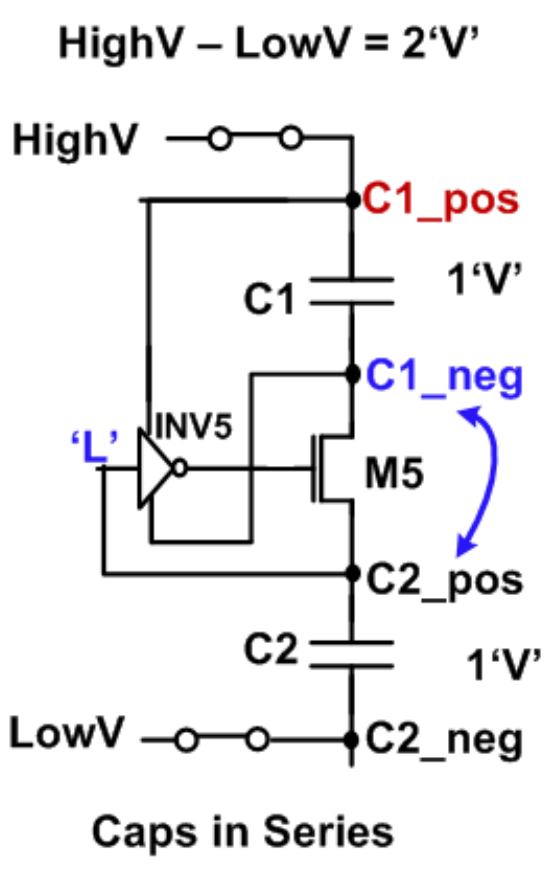
- **Most switches easy to drive**
  - 2 voltage domains:
    - (Vi – Vo)
    - (Vo – GND)
- **M4, M5, and M7 challenging**
  - Experience voltages between the two domains



Switch Driver – M5

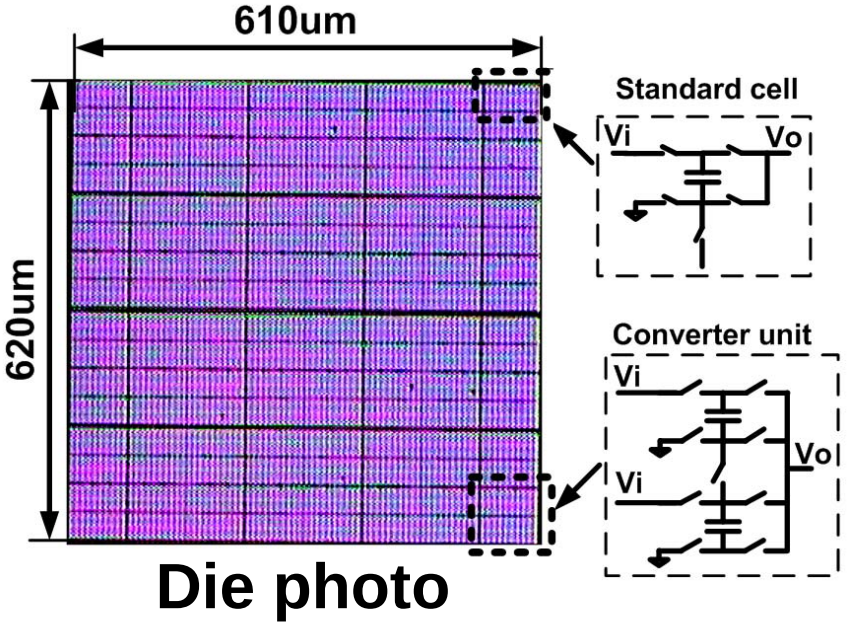






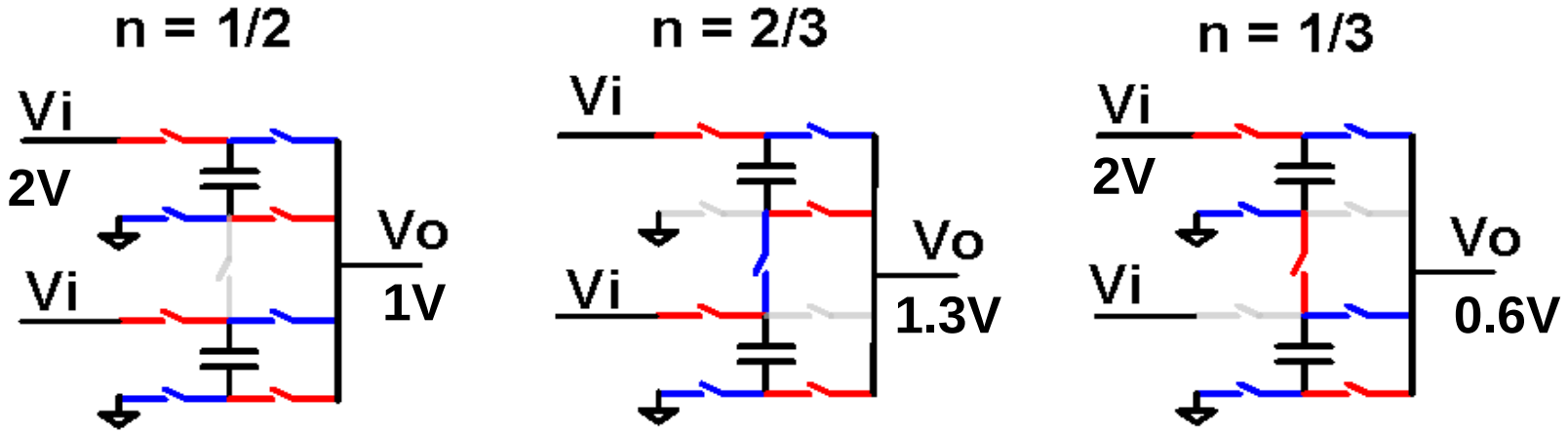
- **"Flying" inverter INV5 powered off of C1**
  - Controlled by top-plate of C2
- **Automatically synchronized by operation of other switches**

SC Converter Prototype

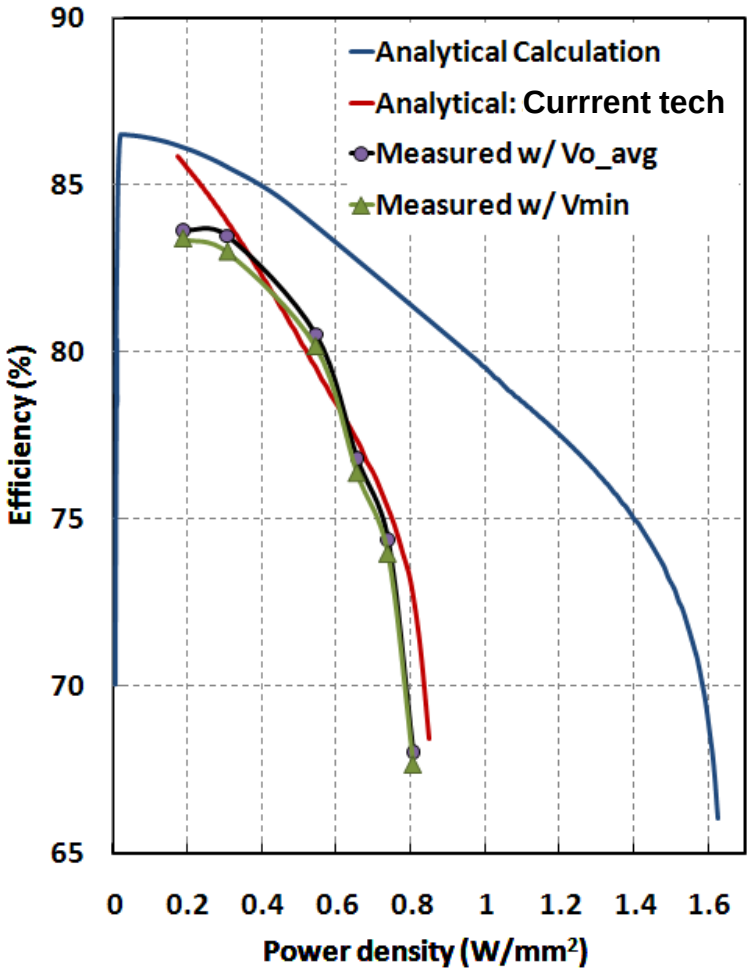


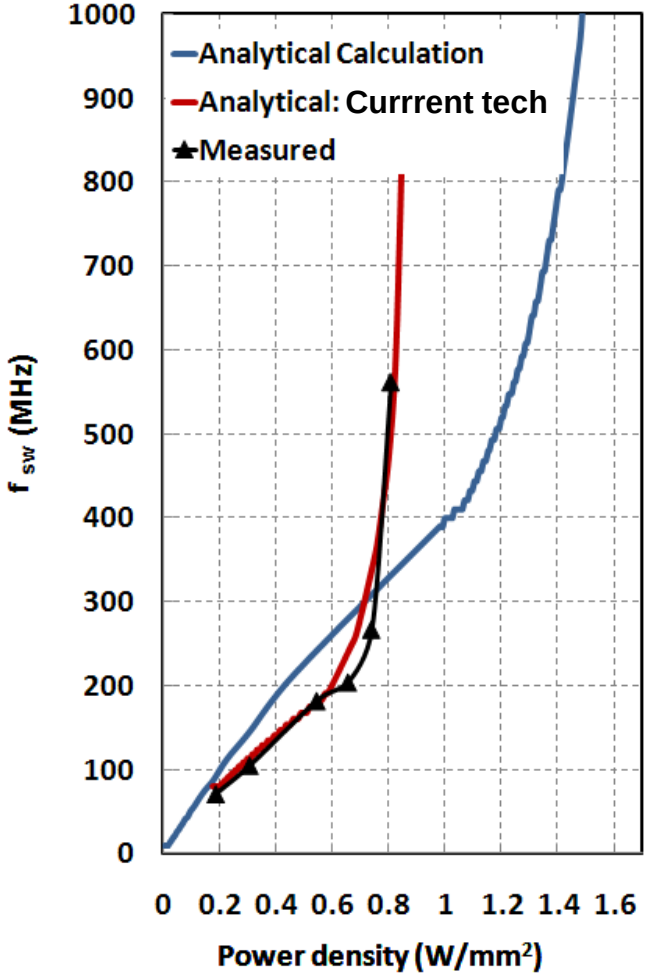
Die photo

- Implemented in 32nm SOI test-chip
- 32-way interleaved
- Supports 0.6V ~ 1.2V from 2V input



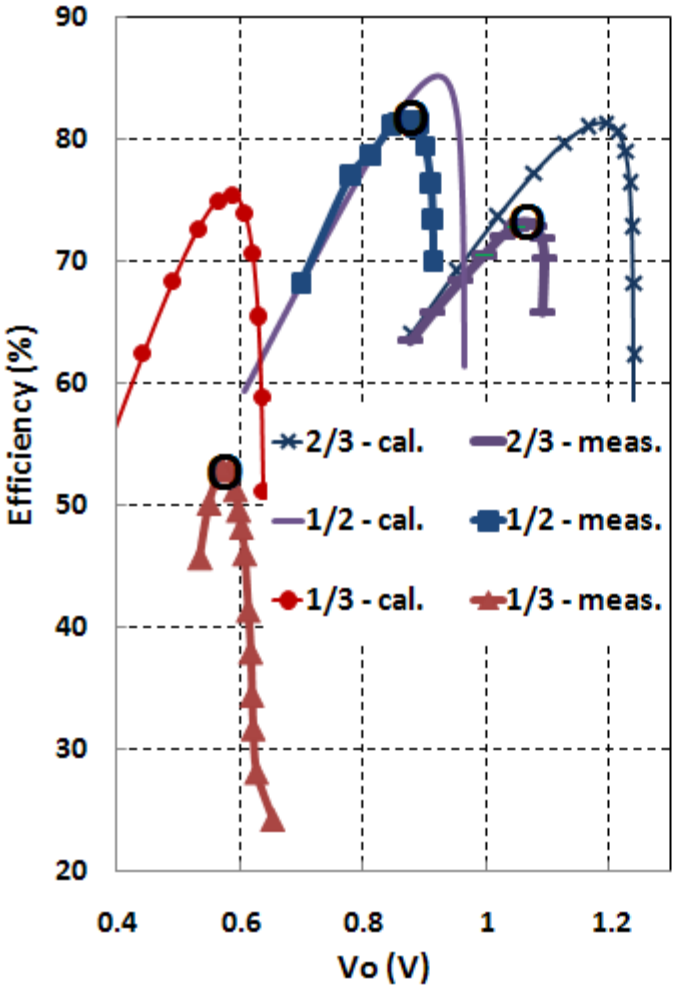
Measured Eff. vs. P-density



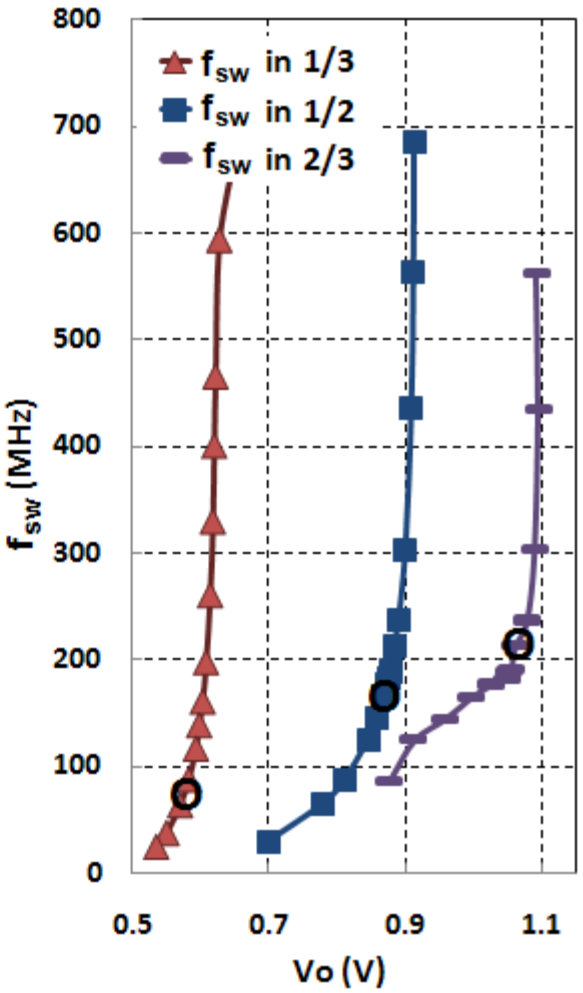


- **Measured in 1/2 mode (Vi = 2V, Vo ≈ 0.88V)**
- **Results promising: 81% efficiency @ 0.55 W/mm²**

Measured Eff. vs. Topologies



Efficiency vs. Vo



f_{sw} vs. Vo

Settings:

Vi = 2V

$R_L \approx 4\Omega$ at

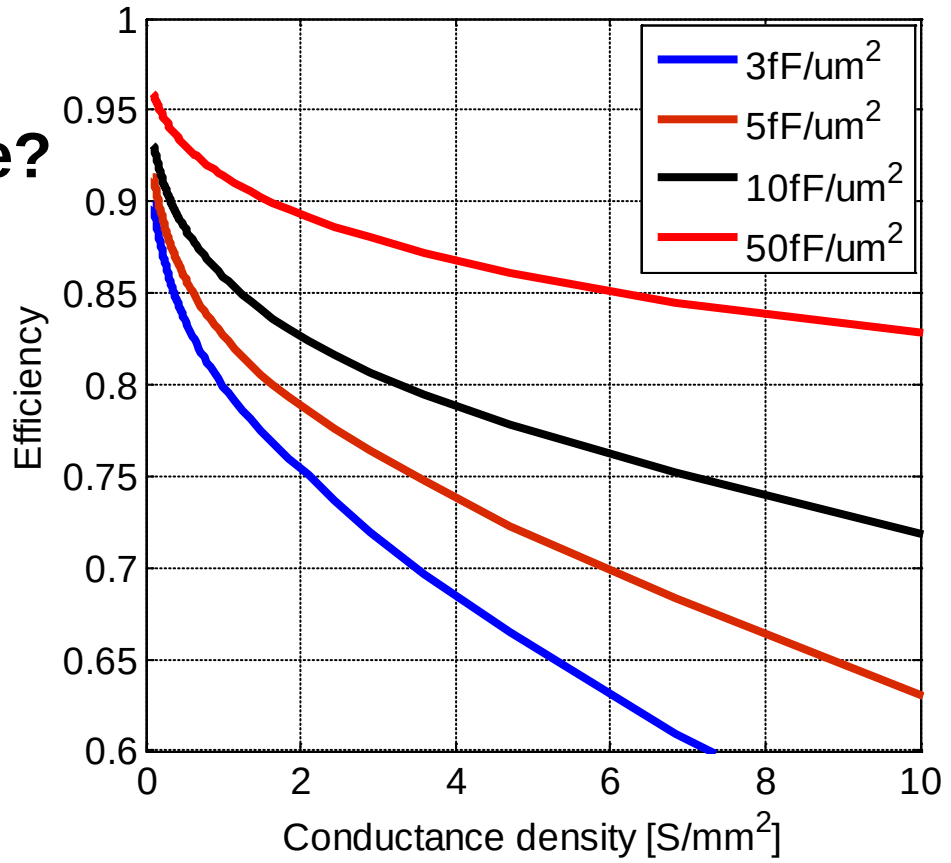
Vo = 0.8V.

How to get 10W/mm²?

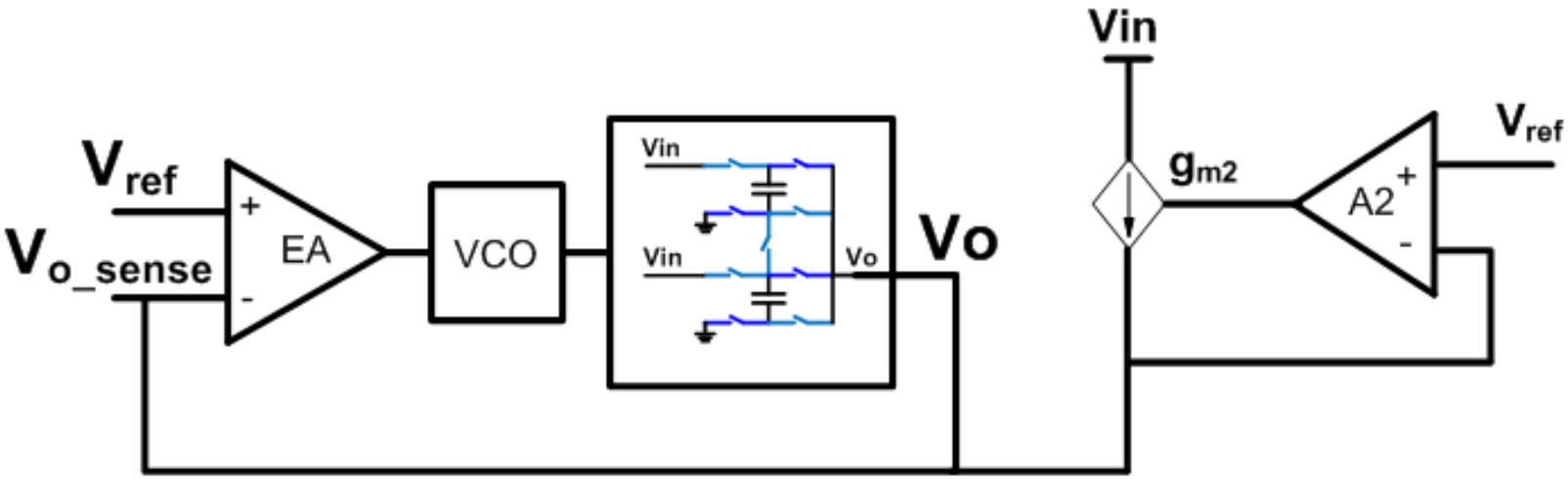
- **If 10W/mm² possible,**
  - Converters will fit in decap of high performance processors

$$\frac{P_{loss}}{P_{Load}} = 3M_{conv,tech}\sqrt[3]{\frac{V_{sw}^2 R_{sw} C_{gate}}{V_o^2 R_L C_{fly}}}$$

- **What does it take to get there?**
  - Effective cap density:
    - 30~50fF/um²
    - 3D packaging
  - New switch technology
    - MEMS
    - Others?



Hybrid Regulator



- **Separate control range**
  - Switched-cap converter controls low frequency (DC) impedance
  - Linear regulator controls high frequency (AC) impedance
    - Only active when needed.

Ref: E. Alon and M. Horowitz, "Integrated Regulation for Energy-Efficient Digital Circuits," *IEEE J. Solid State Circuits*, vol. 43, no. 8, pp. 1795-1807, Aug. 2008.

Conclusions

- **Clear needs for fully-integrated DC-DC converters**
  - Switched–cap: a promising option
- **First demonstration achieves both high power density and high efficiency**
  - In 2:1: 81% efficiency at 0.55W/mm^2
- **Reconfigurable to maintain efficiency over wide output voltage range**
  - >70% efficiency for Vo from ~0.7V to 1.15V
- **Will need close-loop regulation and higher power density.**

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